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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1

of 3

Complete if Known

Application Number	08/801,628
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Filing Date	08 March 2001
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First Named Inventor	Keeth et al.
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Group Art Unit	2818
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Examiner Name	Not yet assigned
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Attorney Docket Number	DB000575-010
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U.S. PATENT DOCUMENTS

Examiner's Initials	Cite No.	U.S. Patent Document Number and Serial (if any)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM/DD/YYYY	Pages, Column, Line, Where Located Page Number of Patent Column, Line
RLT		6,043,118	Suvvarani et al	03/28/2000	438 253
		5,960,455	Bauman	08/28/1999	711 120
		5,838,627	Tomishima et al.	11/17/1998	365 230, C3
		5,677,645	Merritt	10/14/1997	327 536
		5,651,011	Keeth	07/22/1997	435 91, 2
		5,614,859	Onq	03/25/1997	327 333
		5,574,697	Manning	11/27/1996	365 226
		5,557,579	Raad et al.	09/17/1996	365 226
		5,552,739	Keeth et al.	09/03/1996	327 558
		5,526,364	Roohparvar	06/11/1996	714 724
		5,518,360	Keeth	05/21/1996	327 57
		5,481,179	Keeth	01/02/1996	323 315
		5,379,263	Orawa et al.	01/03/1995	365 230, D4
		5,373,227	Keeth	12/13/1994	323 313
		5,266,821	Chem et al.	11/30/1993	263 312
		5,231,605	Lee	07/27/1993	365 201
		5,212,440	Waller	05/18/1993	923 313
		5,193,273	Wright et al.	10/27/1992	824 537
		5,155,704	Walther et al.	10/13/1992	365 201
		4,970,725	McEnroe et al.	11/13/1990	714 25

FOREIGN PATENT DOCUMENTS

[illegible]

Examiner Signature	11. TRAN	Date Considered	10/20/03
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 608. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 15 if possible. ⁶ Applicant is to place a check mark here if English language translation is attached.

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Applicant: PTO/US/CB (6a-20)
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Substitute for form 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	08/801,628
		Filing Date	08 March 2001
		First Named Inventor	Keeth et al.
		Group Art Unit	2818
		Examiner Name	Not yet assigned
Sheet 2 of 3	Attorney Docket Number	DB000575-010	

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and country where published.	T ¹
AK		SUGIBAYASHI ET AL., "A 30-ns 256-Mb DRAM with a Multidivided Array Structure", IEEE Journal of Solid-State Circuits, Vol. 28 (No. 11), (November 1993)	
f		TAGUCHI ET AL., "A 40-ns 64-Mb DRAM with 84-b Parallel Data Bus Architecture", IEEE Journal of Solid-State Circuits, Vol. 26 (No. 11), (November 1991)	
f		KITSUKAWA ET AL., "256-Mb DRAM Circuit Technologies for File Applications", IEEE Journal of Solid-State Circuits, Vol. 28 (No. 11), (November 1993)	
		JEDEC SOLID STATE PRODUCTS ENGINEERING COUNCIL, "Committee Letter Ballot", JC-42.3-95-73, Item #633.13, Arlington, VA (April 1995)	
MT		YOO ET AL., "SP 23.6: A 32-Bank 1Gb DRAM with 1 GB/s Bandwidth", ISSCC96/Session 23/DRAM/PAPER SP 23.6	
f		NITTA ET AL., "SP 23.6: A 1.6GB/s Data-Rate 1Gb Synchronous DRAM with Hierarchical Square-Shaped Memory Block and Distributed Bank Architecture", ISSCC96/Session 23/DRAM PAPER SP 23.6	
		U.S. Patent Application S.N. 08/521,563, entitled IMPROVED VOLTAGE REGULATOR CIRCUIT, filed 8/30/95	
		U.S. Patent Application S.N. 08/668,347, entitled DIFFERENTIAL VOLTAGE REGULATOR, filed 6/26/96	
MT		U.S. Patent Application S.N. 08/460,234, entitled SINGLE DEPOSITION LAYER METAL DYNAMIC RANDOM ACCESS MEMORY, filed 8/17/95	
		U.S. Patent Application S.N. 08/420,943, entitled DYNAMIC RANDOM-ACCESS MEMORY, filed 6/4/95	
AK		U.S. Patent Application S.N. 08/194,184, entitled INTEGRATED CIRCUIT POWER SUPPLY HAVING PIECEWISE LINEARITY, filed 2/8/94	

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PTO/SB/058 (06-00)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	3	of	3
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Complete if Known

Application Number	08/801,628
Filing Date	03/08/2001
First Named Inventor	Keath et al.
Group Art Unit	2818
Examiner Name	Not yet assigned
Attorney Docket Number	DB000575-010

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

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